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EXAMINER CHENG, PETER L.				
ART UNIT 2625		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary

Application No.

10/623,645

Applicant(s)

WANG ET AL.

Examiner

PETER L. CHENG

Art Unit

2625

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date _____

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **NOSE [US Patent Application 2002/0163490 A1]** in view of **LEE [US Patent Application 2003/0132907 A1]** and in view of *prior art* taught by NOSE.

As for claim 2, NOSE teaches *prior art* in which a data driver of a display

[Fig. 10 illustrates an LCD display driver]

forming an image frame by sequentially scanning horizontal lines

[Fig. 12 illustrates the horizontal scanning of image data corresponding to the primary colors, red, green and blue],

the data driver comprising:

**a shift register receiving image data of three primary colors in serial and
outputting the image data of the three primary colors in parallel within each
of scan durations of the horizontal lines**

**[Fig. 11 "shift register section" 163 and "data register section" 164 hold image
data for red, green and blue channels *simultaneously*;**

NOSE cites, "6 bits of R-color gray-scale data DR, 6 bits of G-color gray-scale data DG, and 6 bits of B-color gray-scale data DB all being fed from the display control circuit 13 are held, in parallel, in a data register section 164 being controlled by an output, which is controlled by a horizontal start pulse HSP and a clock signal HCK, fed at each stage in a shift register section 163" **page 2, paragraph 12, lines 1 - 7];**

a sample and hold register acquiring the image data of the three primary colors from the shift register

[Fig. 11 “data register section” 164 and “latch section” 165 correspond to the “sample and hold register”;

NOSE teaches, “The ... gray-scale data DR, DG, and DB” (which are not the same as DR, DG and DB shown in Fig. 3) “being held in parallel in the data register section 164 are transferred collectively to a latch section 165 by a latch signal STB and then are latched therein”; **page 2, paragraph 12, lines 7 – 11];**

However, with respect to the embodiment of the invention for this claim, NOSE does not specifically teach limitations

[1] a first multiplexer receiving the image data of the three primary colors from the sample and hold register and outputting them in a sequence of the primary colors within each of the scan durations of the horizontal lines;

[2] a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the primary colors within each of the scan durations of the horizontal lines;

[3] a digital-to-analog converter for gamma calibration, receiving the image data from the first multiplexer and the gamma reference voltages from

the second multiplexer, and outputting calibrated image signals of the three primary colors;

and [4] a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the primary colors;

Regarding limitation [1], LEE's invention "provides an apparatus and method for driving a liquid crystal display wherein a digital to analog converter part is driven on a time-division basis to increase the number of output channels of the data driving IC while the chip area is not greatly increased or reduced in comparison to the existing chip area, thereby reducing the number of data driving IC's and TCP's"; **page 2, paragraph 23, lines 1 – 8.**

With reference to **Figs. 4 - 6**, LEE teaches

a first multiplexer receiving the image data of the three primary colors from the sample and hold register

[Figs. 4, 5 "latch part" 36 which is controlled by the "shift register part" 34 and Fig. 6 "latch" 46 correspond to the "sample and hold register"; Figs. 4, 5 "mux part" 38 and Fig. 6 "multiplexor" 48 corresponds to the "first multiplexor".

"FIG. 6 illustrates a transmission path of three red (R), green (G), and blue (B) pixel data within the data driving IC shown in FIG. 5"; **page 4, paragraph 57, lines 1 – 3]**

and outputting them in a sequence of the primary colors within each of the scan durations of the horizontal lines

["The multiplexor 48 performs a time-division of the R, G, and B pixel data inputted from the three latches 46 to sequentially supply the time-divided pixel data to a single DAC 50"; **page 4, paragraph 59, lines 1 – 4.**

In this manner, "in the data driving IC ..., the number of DAC's are reduced to at least 1/3 by a time-divisional driving of the DAC part, thereby reducing a space occupied by the DAC part within the IC"; **page 5, paragraph 67, lines 1 - 5];**

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of LEE with those of NOSE by adding a **"first multiplexer receiving the image data of the three primary colors"** from the sample and hold register as this would reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation **[2]**, according to NOSE's first embodiment shown in **Fig. 3**, NOSE teaches

a second multiplexer outputting gamma reference voltages for the three primary colors in the sequence of the primary colors within each of the scan durations of the horizontal lines;

Fig. 3 "RGB switching reference gray-scale voltage producing circuit" **4** contains a multiplexer consisting of multiplexers **M1, M2, ..., M10** which is controlled by a common signal **SL**.

NOSE cites," voltages obtained by selecting from voltages V0R, V0G, V0B, ..., V9R, V9G, and V9B which are obtained by dividing a reference voltage V_{REF} using a voltage dividing circuit for a R color (DR), a voltage dividing circuit for a G color (DG), and a voltage dividing circuit for a B color (DB), respectively, for every color of the R, G, and B colors in accordance with a selection control signal SL using MPXs (multiplexers) M1, M2, ..., M9, and M10, are output, through voltage followers B1, B2, ..., B9, and B10, as reference gray-scale voltages V0, V1, V1, ..., V8, and V9"; **page 6, paragraph 82, lines 2 – 12.** "Each of the MPXs M1, M2, ..., M9, and M10 selects a corresponding voltage in response to the selection control signal SL being output in synchronization with the selection of the scanning line 21 for each of the R, G, and B colors and outputs it as the reference gray-scale voltage to the signal line driving circuit 6"; **page 6, paragraph 82, lines 15 – 20.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of a "**gamma multiplexer**" or "RGB switching reference gray-scale voltage producing circuit" with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation [3], according to NOSE's first embodiment shown in Fig. 3, NOSE teaches

a digital-to-analog converter for gamma calibration, receiving the image data from the first multiplexer and the gamma reference voltages from the second multiplexer, and outputting calibrated image signals of the three primary colors;

Fig. 3 "DAC" **62** is a digital-to-analog converter which receives the image data from the sample-and-hold register ("data register section" **64** and "latch section" **65**) after the data is passed through a "level shift section **66**" [page 6, paragraph 83, lines 14 – 15]. The DAC reference voltage, for each of the three primary colors - red, green, and blue, is provided through multiplexer **61**. "Gray-scale data D1, D2, and D3 having been transferred to the DAC **62** undergo the gamma correction based on the set of the reference gray-scale voltages V0 to V4 and the set of the reference gray-scale voltages V5 to V9 fed from the MPX **61**, and at the same time, causes a D/A converted signal

voltage to be generated which is output through the voltage followers F1, F2, ..., F639, and F640 to each of the corresponding signal lines 22"; **page 6, paragraph 83, line 15 – page 7, paragraph 83, line (starting on page 7) 6.**

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of a "**digital-to-analog converter for gamma calibration**" with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Regarding limitation [4], according to NOSE's first embodiment shown in **Fig. 3**, NOSE teaches

a buffer receiving the calibrated image signals from the digital-to-analog converter and outputting the calibrated image signals in the sequence of the primary colors;

Fig. 3 "voltage followers" **F1, F2, ..., F640** correspond to the "buffer receiving the calibrated image signals from the digital-to-analog converter".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine NOSE's teachings of a "**buffer receiving the calibrated image**

signals from the digital-to-analog converter” with the teachings of ZAVRACKY (i.e., the addition of a multiplexer between the sample-and-hold register and digital-to-analog converter) and the *prior art* taught by NOSE so as to reduce the number of “digital-to-analog” and “buffer” functional blocks resulting in lower hardware cost.

Response to Arguments

5. Applicant's arguments filed **11/18/2008** have been fully considered but they are moot in view of the new grounds of rejection.

However, with respect to applicant's argument

that NOSE's "register section 164 and latch section 165 do not teach the sample and hold register of the present invention

and

Nose fails to disclose a multiplexer of any sort that would receive "image data of three primary colors" from register 164 and latch 165

have been considered.

In reply:

Regarding the first argument, in addition to disclosing that the data register section 164 outputs the RGB data in parallel to the latch section 165, NOSE teaches that the “data register section 164” is controlled by an output of the “shift register section 163”. The output of the shift register section 163 is controlled by a horizontal start pulse HSP and a clock signal HCK”; **page 2, paragraph 12, lines 1 – 7.**

As noted in this and the previous actions, the instant application’s **shift register receiving image data of three primary colors in serial and outputting the image data of the three primary colors in parallel within each of scan durations of the horizontal lines**

corresponds to the “shift register section” **163** and “data register section” **164** shown in **Fig. 11**. The “shift register section” produces “timed outputs” based on the “clock signal HCK” and the “horizontal start pulse HSP”. A single “timed output” causes the “data register section” to store a pixel/s corresponding bits DR (6 bits for red), DG (6 bits for green) and DB (6 bits for blue). Since a single “timed output” occurs for every period of clock signal HCK, RGB data for all 1920 (i.e., 3 x 640) pixels is eventually stored in the “data register section”.

In this way, the serial data streams DR[0:5], DG[0:5] and DB[0:5] are shifted into the “data register section”. (Please note that each DR[0:5], DG[0:5] and

DB[0:5] may be considered as a separate serial data bus with each of the 6 signals contained within each serial data bus as a serial data line.) Once all RGB data for an entire horizontal line has been shifted serially into the "data register section", it is transferred in parallel to the "latch section" **165**. Once all RGB data for an entire horizontal line has been latched in the "latch section", the process of shifting the next horizontal line can begin while the latched RGB data for the present horizontal line is "level-shifted", converted to analog and displayed.

Furthermore, the hardware configuration taught by LEE and as shown in **Fig. 4** illustrates a "shift register part" **34** which corresponds to the instant application's "shift register" shown in **Fig. 4**, a "latch part" **36** which corresponds to the instant application's "sample and hold" shown in **Fig. 4**, a "mux part" **38** which corresponds to the instant application's "MUX" shown in **Fig. 4**, a "DAC part" **40** which corresponds to the instant application's "DAC" shown in **Fig. 4**, and a "Demux part" **42** which corresponds to the instant application's 3 switches for R, G and B analog signals shown in **Fig. 4**.

Clearly, the configurations taught by both NOSE and LEE serve to shift data into a register by means of a "clock signal" and "start pulse" and to latch (or hold) the data in a register.

Regarding the second argument, the Examiner concurs that the configuration illustrated in **Fig. 11** does not show a multiplexer that receives RGB data from a "sample and hold register". However, as noted in the claim rejection, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of LEE with those of NOSE by adding a "**first multiplexer receiving the image data of the three primary colors**" from the sample and hold register as this would reduce the number of "digital-to-analog" and "buffer" functional blocks resulting in lower hardware cost.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 571-272-7440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/King Y. Poon/
Supervisory Patent Examiner, Art Unit 2625

plc
December 8, 2008